Applicants have amended their title in light of the requirement in Item 1 on page 2 of the Office Action mailed August 9, 2000. In view of the submitted new title, it is respectfully submitted that the requirement for a new title has been satisfied.

Applicants have amended their claims in order to further clarify the subject matter of the present invention. Specifically, Applicants have canceled previously considered claims 7 and 8 (directed to a semiconductor device) without prejudice or disclaimer. In addition, Applicants have amended each of claims 1 and 2 to clarify the trench portion; to recite the step, after burying the buried insulating film, of oxidizing the semiconductor substrate; to recite the step of eliminating the oxidation prevention film formed on the semiconductor substrate; and to recite the step, after this step of eliminating the oxidation prevention film, of forming a gate oxidation film.

In addition, Applicants have amended each of claims 4, 5 and 9 to clarify the trench portion or portions; and to recite the additional step, after the step of oxidizing the semiconductor substrate, of forming a gate oxidation film.

In connection with the amendments to the previously considered claims, including formation of the gate oxidation film, note, for example, Fig. 3 of Applicants' original disclosure.

In addition, Applicants have added new claims 10-17 to the application. Of these newly added claims, claims 10 and 15 are independent claims, and each is directed to a method of

fabricating a semiconductor device. Claim 10 recites the processing steps recited in previously considered claim 1; and also recites the processing step, after burying the buried insulating film, of increasing a curvature of an upper end portion of the trench. Claim 15 recites the processing steps recited in previously considered claim 1, and also recites that the trench portion formed in the semiconductor substrate is oxidized so as to increase a curvature of an upper end portion of the trench.

Claims 11 and 17, dependent respectively on claims 10 and 15, respectively recites that the increasing the curvature includes thermally oxidizing the upper end portion of the trench, and recites that the oxidizing is a thermal oxidation so as to increase the curvature. Claims 12 and 16, dependent respectively on claims 10 and 15, respectively recites that the increasing the curvature includes forming bird's beaks at the upper end portion of the trench; and recites that the oxidizing of the trench portion forms a bird's beak at the upper end portion of the trench, so as to increase the curvature. Claims 13 and 14, each dependent on claim 10, respectively recites that the increasing of the curvature is performed to provide an angle, within a specified range, between the circuit formation surface of the semiconductor substrate and a side surface of the semiconductor substrate forming the trench; and recites that the increasing the curvature is performed after removing the buried insulating film.

In connection with these newly added claims, note, for example, Fig. 3 of Applicants' original disclosure, together with the description on pages 6-9, and on pages 11-15, of Applicants' specification.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references as applied by the Examiner in rejecting claims formerly in the application, that is, the teachings of the U.S. patents to Fazan, et al., No. 5,433,794, and to Perera, No. 5,786,263, and European Patent Application No. 459396 (Miyashita), under the provisions of 35 USC 102 and 35 USC 103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including, inter alia, wherein, after forming the trench and after burying the buried insulating film into the trench so oxidized, the semiconductor substrate is oxidized; and, after eliminating the oxidation prevention film formed on the semiconductor substrate, a gate oxidation film is formed. Note claims 1 and 2.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including the forming of the specified trenches, oxidizing trench portions and burying a buried insulating film into the trenches so oxidized, and oxidizing the semiconductor

substrate after the buried insulating film formed on the oxidation prevention film is removed; and wherein after this oxidizing of the semiconductor substrate after the buried insulating film has been removed, the step of forming the gate oxidation film. See claims 4 and 5; note also claim 9, reciting the step of performing a second oxidation to selectively oxidize an opening side of the completely filled trench regions in the substrate, and, after performing this second oxidation, forming a gate oxidation film.

Furthermore, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor device as in the present claims, including forming the trench and oxidizing the specified trench portion, and burying a buried insulating film into the trench so oxidized, and wherein after burying the buried insulating film a curvature of an upper end portion of the trench is increased. See claim 10.

In addition, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested such method of fabricating a semiconductor device as in the present claims, including the trench formation and trench portion oxidizing, and burying a buried insulating film into the trench so oxidized, and wherein the oxidizing of the trench portion is performed so as to increase a curvature of an upper end portion of the trench. See claim 15.

Moreover, it is respectfully submitted that the teachings of the applied references would have neither disclosed nor would have suggested the other aspects of the present invention as in the remaining, dependent claims, including (but not limited to) wherein the step of increasing the curvature includes thermally oxidizing the upper end portion of the trench (see claim 11; note also claim 17); and/or wherein the increasing of the curvature includes forming bird's beaks at the upper end portion of the trench (see claim 12; note also claim 16); and/or wherein the increasing the curvature is performed such that the specified angle is within a range of greater than 90° and less than 180° (see claim 13); and/or wherein the increasing the curvature is performed after removing the buried insulating film (see claim 14).

The invention as presently claimed in the above-identified application is directed to a method of manufacturing a semiconductor device having a trench isolation structure. A so-called "trench isolation structure" made by a selective oxidation method, which forms trenches extending into the substrate from the substrate surface and then selectively oxidizes the trenches to form a thermal oxide film, has been employed as the insulation/isolation structure of semiconductor devices, as described in the paragraph bridging pages 1 and 2 of Applicants' specification.

In the trench isolation structure, end points (corner points) essentially exist near the trench upper end portion of the semiconductor substrate. A stress concentration field is formed near the end points. Because such a stress

concentration field is formed, the shape of the substrate, particularly near the trench upper end portion, is oxidized in some cases into a pointed shape having an acute angle, as shown in Fig. 1C of Applicants' disclosure. If such an acute angle portion 4 remains on the semiconductor surface, however, concentration of electric field occurs at this portion during the circuit operation and deteriorates the breakdown voltage characteristics of transistors, capacitors, etc., formed utilizing such substrate. See the paragraph bridging pages 3 and 4 of Applicants' specification.

Against this background, Applicants provide a process wherein trench isolation can be utilized, without causing deterioration of breakdown voltage characteristics of transistors and capacitors utilizing the substrate with the trench isolation structure, while providing semiconductor devices having a high reliability. Moreover, Applicants fabricate such structure utilizing a relatively simple technique.

Applicants have found that the desired structure can be achieved by preventing a substrate shape in the proximity of the upper end portion of the device isolation trench from becoming an acute angle; and, by the present invention, provide simple techniques for preventing such acute angle. Specifically, according to the present invention, Applicants provide various processing procedures which can easily and effectively increase curvature of an upper end portion of the trench, so as to prevent the aforementioned acute angle. For example, and specifically, according to the present invention,

after burying the buried insulating film, the semiconductor substrate can be oxidized. Moreover, the semiconductor substrate can be oxidized after the buried insulating film formed on the oxidation prevention film is removed. Moreover, more generally, after burying the buried insulating film, a curvature of an upper end portion of the trench can be increased. Furthermore, the trench portion formed in the semiconductor substrate can be oxidized, so as to increase a curvature of an upper end portion of the trench. This prevention of the acute angle can be achieved, for example, by thermal oxidation of the upper end portion of the trench; e.g., by forming bird's beaks at the upper end portion of the trench.

Fazan, et al. discloses formation of trenches useful in isolating active regions on a semiconductor substrate. The process of producing the trenches is begun with standard trench-forming steps, but further forms spacers around the periphery of the trench. These spacers then combine with the isolation material disposed in the trench to form a dome-like structure over the trench. The dome-like structure extends over the peripheral edges of the trench thereby limiting the effect of the corners. See column 1, lines 41-47. Note also column 1, lines 37-40 and 49-51; column 2, lines 38-42; column 3, lines 3-7, 24-27, 41 and 42, and 51-54; and column 3, line 66 to column 4, line 2.

Note that Fazan, et al. discloses forming <u>additional material</u> to provide a dome-like structure over the trench. It is respectfully submitted that this reference does not

disclose, nor would have suggested, oxidation of the substrate after burying the buried insulating film, particularly in combination with the further steps of removing the buried insulating film, eliminating the oxidation prevention film, and (after this eliminating) forming a gate oxidation film, as in present claim 1.

That is, it is respectfully submitted that according to Fazan, et al. there is no disclosure, nor would there have been any suggestion, of the step of oxidizing after burying the buried insulating film, with a later step of forming a gate oxidation film; and/or wherein, for example, the curvature of an upper portion of the trench is increased after burying the buried insulating film, or wherein oxidation of the trench portion is performed so as to increase a curvature of an upper end portion of the trench, as in various of the present claims. In this regard, it is again emphasized that according to Fazan, et al., additional structure is provided extending above the surface of the trench, to avoid the corner effect.

Perera discloses a method for forming a trench isolation structure in an integrated circuit. The method includes anisotropically etching a first portion of a semiconductor substrate, using standard etching techniques to form a trench having a trench sidewall 24 and a trench bottom 26 (see Fig. 3). After formation of the trench, the photoresist mask used for forming the trench is removed using standard photoresist stripping techniques. A silicon layer 28 is then formed which overlies a remaining portion 16 of an oxidation resistant

layer 15 and lies within trench 22; and this silicon layer 28 is then completely oxidized to form a first dielectric layer 30 that lies within trench 22 and overlies the remaining portion 16 of oxidation resistant layer 15, first dielectric layer 30 having a thickness that is insufficient to fill trench 22 (note Figs. 4 and 5). The first dielectric layer 30 is then isotropically etched (see Fig. 6) to form an etched dielectric layer 32 that lies within trench 22 and overlies the remaining portion 16 of oxidation resistant layer 15. A portion of first dielectric layer 30 is removed to form etched dielectric layer 32 that has a surface topography. A second dielectric layer 34 is then formed overlying etched dielectric layer 32 and substantially filling trench 22 (see Fig. 7). A portion of the second dielectric layer 34 and a portion of etched dielectric layer 32 are then selectively removed to expose the remaining portion 16 of oxidation resistant layer 15, and to form trench plug 36 within trench 22 (see Fig. 8). In connection with this description in Perera, note from column 2, line 28 to column 3, line 47.

It is respectfully submitted that Perera does not disclose, nor would have suggested, <u>increasing curvature of an upper end portion of the trench</u>, as in various of the present claims. Moreover, it is noted that according to various of the present claims, oxidation is performed <u>after</u> burying the buried insulating film, with a step, <u>after eliminating the oxidation prevention film</u>, being performed to form the gate oxidation film. It is respectfully submitted that the step of forming the gate oxidation film, which forms a relatively thin

film, would not increase curvature of an upper end portion of the trench, e.g., to prevent the acute angle so as to avoid current leakage. Thus, it is respectfully submitted that Perera would have neither disclosed nor would have suggested the presently claimed subject matter.

Even taking the teachings of Perera and Fazan, et al., in combination, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including wherein the second oxidation to selectively oxidize an opening side of the completely filled trench regions in the substrate is performed, with a gate oxidation film being formed <u>after performing this second oxidation</u>.

Miyashita, et al. discloses a semiconductor device having device isolation made by a trench formed in a semiconductor substrate, and a method of fabricating this device. The method includes a first step of forming a device-isolating trench, with a taper at an upper portion thereof, in a semiconductor substrate; and a second step of forming an oxide film on an inner wall of the trench and a surface of the substrate near the trench by an oxidizing method. Note the paragraph bridging columns 1 and 2 of this patent. See also column 2, lines 54-58; column 3, lines 4-12, 17-25, 33-39 and 42-46; and column 4, lines 39-54.

Specifically, Miyashita, et al. discloses fabricating an area of large curvature in an upper portion of the trench, by combining isotropic and anisotropic etching. Even taking the teachings of Miyashita, et al. in combination with the

teachings of Fazan, et al., or in combination with the teachings of both of Fazan, et al. and Perera, it is respectfully submitted that the combined teachings of these references would have neither disclosed nor would have suggested the present invention, including the step of oxidizing, e.g., separate from the step of forming the gate oxidation film; and/or wherein, after burying the buried insulating layer, a curvature of an upper end portion of the trench is increased; and/or the oxidizing to increase the curvature of an upper end portion of the trench, or the other aspects of the present invention as discussed in the foregoing. These techniques provide advantages that by use of a relatively simple technique of oxidation acute angles at upper end corners of the trench can be avoided, so as to prevent increase of leakage current or drop of breakdown voltage characteristics resulting from the field concentration near the end portion of the gate electrode, and can improve electrical reliability of a transistor formed on the substrate using the trench isolation.

In view of the foregoing comments and amendments to the specification and claims, reconsideration and allowance of all claims remaining in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit

Account No. 01-2135 (Case No. 500.36904X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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